Abstract of the Disclosure

A memory tester tests a random access memory device under test (DUT) comprising addressable rows and columns of memory cells, and provides a computer with enough information to determine how to efficiently allocate spare rows and columns for replacing rows and columns containing defective memory cells. During a test the memory tester writes a "fail" bit into each address of an error capture memory (ECM) to indicate whether a correspondingly addressed memory cell of the DUT is defective. The tester also includes a set of programmable area fail counters, each for counting of the number of memory cells within a separately selected area of the memory's address space. After the test, the computer processes the counts to determine whether it needs to allocate the spare rows and columns and, in some cases, to determine how to allocate the spare rows and columns. When it cannot allocate spare rows and columns on the basis of the counts alone, the computer commands the tester to read the fail bits in selected areas of the ECM's address space to determine the addresses of the defective memory cells and to supply those addresses to the computer to enable it to determine how to allocate spare rows and columns.